THE DESIGN AND PERFORMANCE OF LARGE SIGNAL DISTRIBUTED MICROWAVE AMPLIFIERS

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ABSTRACT

Large signal models of microwave power MESFETS have been developed. The models match closely measured D.C. and R.F. characteristics of the device. The complete distributed microwave amplifier was simulated using a non-linear simulation program. Three circuits were built and results show good agreement with predicted performances. Power outputs up to 0.7 Watt were obtained over the range 2-6 GHz using 3 MESFETs per circuit. The non-linear simulation was able to predict the dynamic range, the power gain, fundamental and harmonic power outputs to a reasonable degree of accuracy.

1. MESFET LARGE SIGNAL MODEL

The large signal model used is shown in Figure 1. This is a complete D.C. and R.F. model that is capable of predicting the performance of the device accurately (1). The parameters of the model (VT, α, β, λ, ε, ξ, δ, γ, Rs and Rd) are optimised to fit the measured D.C. current-voltage characteristics. The remaining circuit elements (Rg, Lg, Cgd, Cgs, Rf, Cf, Rio, Cds, Ld and Ls) are optimised to fit the measured R.F. characteristics over the required frequency range 2-12 GHz and at three different bias conditions which span the D.C. I/V characteristics. An example of the D.C. fit obtained for an HMF-1200, 0.5 Watt power MESFET is shown in Figure 2. Figures 3a and 3b show the R.F. S-parameter fit at two different bias conditions. It is evident from these results that the derived models fit the measured results very well.

2. AMPLIFIER DESIGN AND SIMULATION

Three different amplifiers were designed using the low frequency design procedure of Niclas et al. (2). The three amplifiers provided a total gate periphery of 2400 μm, 1800 μm and 3600 μm respectively. In the first design (PAMP1) it was assumed that the power at the drain of each FET would increase along the drain line towards the output which would imply that the last FET should provide the largest output power at its drain. The second configuration assumed equal power output along the drain line from equal 600 μm gate peripheral MESFETs. For obvious reasons the output power from the third design was assumed greater than the second.

Figure 4 shows the topology of the distributed power amplifier designs. In the first design (PAMP1) a half Watt FET was placed nearest the output, the other FET stages were quarter Watt FETs. Equal quarter Watt and half Watt FET stages were considered in the second and third designs (PAMP2 and PAMP3) respectively.

As an example of the design procedure Table I shows the initial values of transmission lines and impedances obtained for PAMP1. These values were converted to microstrip line equivalents on alumina of dielectric constant 9.8 and were optimised using the linear CAD program 'Touchstone' for a flat small-signal gain response at one bias point, Vgs = -1.62V, Vds = 7V, Ids = 146 mA. The final microstrip values obtained are shown in the table.

The amplifiers were then simulated using the non-linear simulation program ANAMIC (3,4) developed at Kent. The results of the simulation will be compared to the measured results in Section 3.

3. PRACTICAL IMPLEMENTATION AND RESULTS

All three amplifiers were implemented. Only the results of amplifier PAMP1 will be shown here for lack of space. Figure 5 shows a photograph of the designed amplifier using 2 HMF-0600 MESFETs in the first two stages and an HMF-1200 in the final stage. The circuits were realised on 0.025" alumina, nichrome layered over gold to realise integral resistors. Two laser cut substrates 12×9 mm forming the respective gate and drain circuits were epoxied onto an Au plated tungsten copper carrier, ridged in the centre. From the photograph it can be seen that the FETs were mounted on the carrier as close as possible to the gate circuit to reduce bondwire inductance. The carrier ridge has a twofold purpose of providing D.C. and R.F. ground (via 100 pF chip capacitors) and to dissipate heat generated by the FETs.

The measured and 'Touchstone' calculated small signal gain response are shown in Figure 6. The power output of PAMP1 over 2 to 6 GHz

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is shown in Figure 7 and the measured and calculated harmonic power output is shown in Figure 8. Table II compares the measured and calculated power output of amplifiers PAMP1 and PAMP2 at 4 GHz input frequency. It is evident that the results of the simulation are in very good agreement with the measured results.

4. SUMMARY

Non-linear equivalent circuit models were derived for a 0.25W and 0.5W power MESFET from measured D.C. and S-parameter data at different bias conditions. The modelled results showed a very good fit to measured characteristics.

Three distributed power amplifiers were designed using initial values from the low frequency design approach of Niclas. Using the S-parameters of the FETs at one bias point, the designs were optimised for a flat small signal gain response with a linear CAD program 'Touchstone', and the measured results showed reasonable agreement with calculated values.

The complete distributed amplifier, simulated using a non-linear program developed at Kent University and using the derived non-linear equivalent circuit models showed good agreement with measured results of output harmonic power and gain. A summary of the overall results of all three amplifiers is given in Table III.

The designs included a particular example (PAMP1) showing a novel approach assuming the final FET stage to have the largest peripheral gate width, hence it was assumed capable of producing a larger power output at its drain terminal. The other designs followed a strategy of using conventional equal gate peripheral devices. The former was capable of producing a higher output power at a greater efficiency than the latter cases. This emphasises the approach of using the largest peripheral device at the last stage in a hybrid distributed power amplifier. The output power achievable by distributed power amplifiers can be greater than conventionally designed single ended or balanced amplifiers at the cost of using a greater number of FETs and at a higher DC power consumption. The advantages of tailoring power devices in the topology of the distributed amplifier, in the manner of PAMP1 can be seen as twofold.

Firstly the DC power required is less by using only one high power FET stage as the final stage rather than equal high power FET stages. This will reduce the problem of thermal heat generated by the amplifier and increase the reliability. Secondly the overall cost of the amplifier will be reduced by using only one high power rated FET, and lower power rated FETs in the remaining stages.

It is possible to combine this approach with the concept of capacitively coupled FET gate inputs in order to increase the achievable power output (5,6). By using series capacitors at the input to each FET, the total gate periphery can be increased and hence a larger power rated FET can be used as the final stage of a distributed power amplifier.

5. ACKNOWLEDGEMENTS

The authors would like to thank Plessey Microwave Ltd., Towcester, U.K., for their help in the manufacture of the circuits.

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Table I: 3-Stage Distributed Power Amplifier Design 1

Amplifier PAMP1 - values refer to Figure 3

FET1 = HMF0600
FET2 = HMF0600
FET3 = HMF1200

Element	Value	Microstrip dimensions Original	Optimised
Fc	7.00 GHz	7.00 GHz	
R1	50.00 Ohms	50.00 Ohms	30.00 Ohms
R2	252.00 Ohms	252.00 Ohms	300.00 Ohms
L1	19.16°	0.95 mm	0.63 mm
L2	38.32°	1.90 mm	2.20 mm
L3	30.29°	1.50 mm	1.37 mm
L4	11.13°	0.55 mm	1.00 mm
L5	42.30°	2.08 mm	0.00
L6	42.30°	2.08 mm	4.22 mm
L7	24.10°	1.18 mm	4.00 mm
Z1,2,3,4	110.00 Ohms	0.05 mm	0.096 mm
Z5,6,7	100.00 Ohms	0.08 mm	0.10 mm

Table II:

Measured and Calculated Fundamental Output Power of PAMP1 and PAMP2 at 4 GHz

PAMP1
Freq = 4 GHz

Input Power	Output Power Meas.		Output Power Calc.		Power Gain Meas.	Power Gain Calc.
dBm	dBm	W	dBm	W	dB	dB
5	12.6	0.018	14.8	0.030	7.6	9.8
10	17.4	0.055	19.8	0.095	7.4	9.8
15	22.0	0.160	23.9	0.245	7.0	8.9
20	23.9	0.246	25.2	0.331	3.9	5.2
25	24.9	0.310	26.6	0.457	0.1	1.6
30	25.7	0.375	28.8	0.758	-4.3	-1.2

PAMP2
Freq = 4 GHz

Input Power	Output Power Meas.		Output Power Calc.		Power Gain Meas.	Power Gain Calc.
dBm	dBm	W	dBm	W	dB	dB
5	13.5	0.022	14.1	0.026	8.5	9.1
10	18.4	0.069	17.1	0.051	8.4	7.1
15	23.2	0.209	20.1	0.102	8.2	5.1
20	26.5	0.447	23.4	0.291	6.5	3.4
25	26.6	0.457	26.9	0.490	0.1	1.9

Table III:

Summarised Power Amplifier Results

	PAMP1	PAMP2	PAMP3
Small-signal gain	8 ±4dB	8±1dB	8±1.5dB
Power at 1dB gain compression 2 to 6 GHz	22.5±4dBm	24±1.5dBm	25.5±3dBm
Maximum Saturated Power Output	28.3 dBm	26.6 dBm	29.5 dBm
Maximum Input at 1dB Gain Compression	17 dBm	17 dBm	17 dBm
DC Power	1.8 W	2.6 W	4.7 W
Power added efficiency 2 to 6 GHz	6.8%	7.7%	6.5%
2nd Harmonic Power	9.0 dBm	7.0 dBm	8.0 dBm
3rd Harmonic Power	-2.0 dBm	-16 dBm	-8 dBm

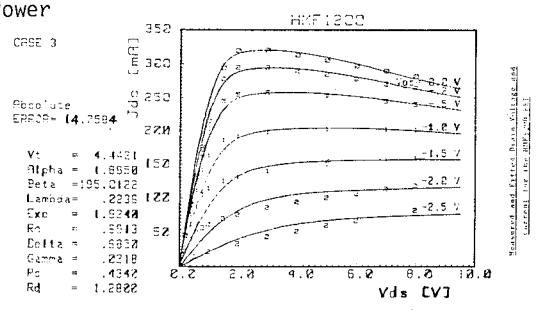


Fig. 2: Measured and Fitted Drain Current and Voltage Characteristics for HMF1200 Power MESFET

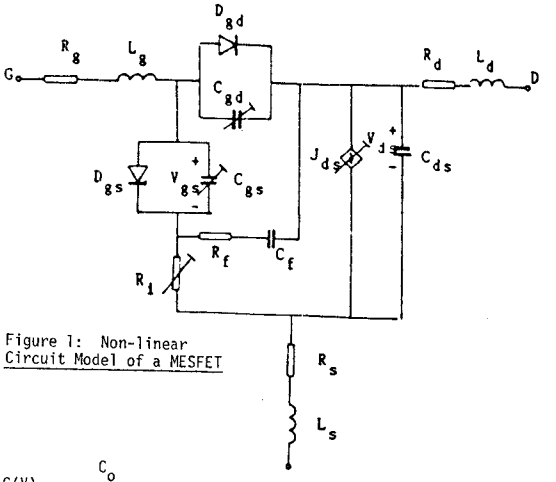


Figure 1: Non-linear Circuit Model of a MESFET

$$C(V) = \frac{C_o}{(1-V/V_{bi})^{\frac{1}{2}}}$$ (all non-linear capacitors)

$$J(V) = J_o(\exp(V/V_T) - 1)$$ (diode non-linear current)

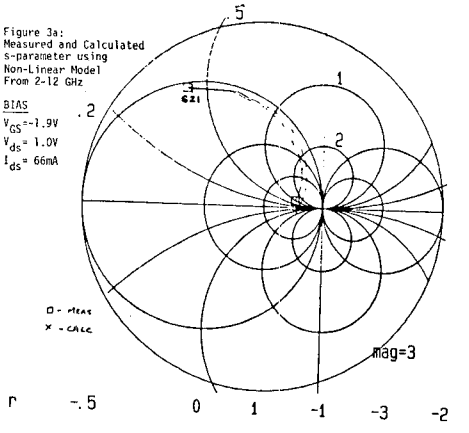
$$R_i(V_{gs}) = R_{io}(1-V_{gs}/V_R)$$

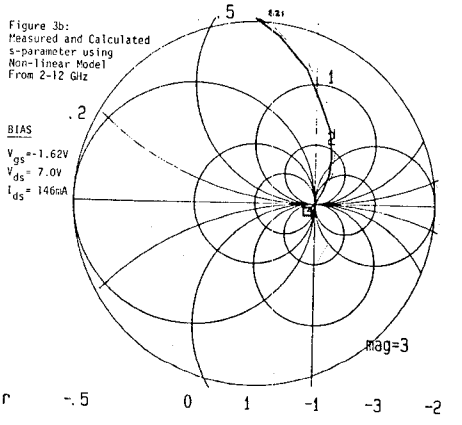
$$V_T = n\ kT/q$$ (threshold voltage)

$$J_{ds}(V_g,V_{ds}) = \beta T(V_g)^{\epsilon}(1+\lambda V_{ds})\tanh(\alpha V_{ds} D(V_g))\,Gunn(V_g,V_{ds})$$

$$D(V_g) = T(V_g) = 1+V_g/V_t$$

$$Gunn\ (V_g,V_{ds}) = 1+pe^{-\gamma[(V_{ds}-\delta)T(V_g)^2]^2}$$





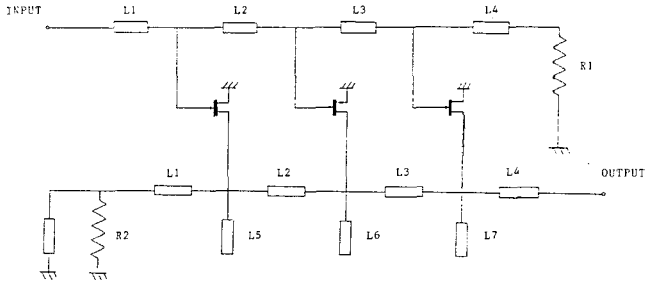


Figure 4: 3-Stage Distributed Power Amplifier

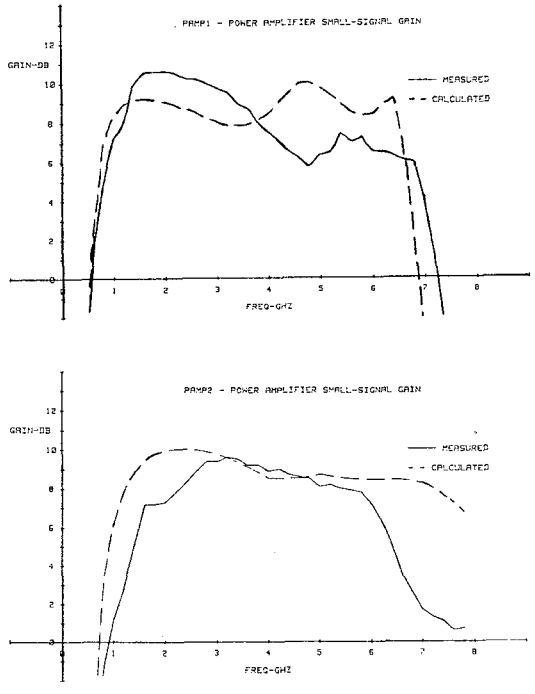


Figure 6: Small-Signal Gain of the Distributed Power Amplifier

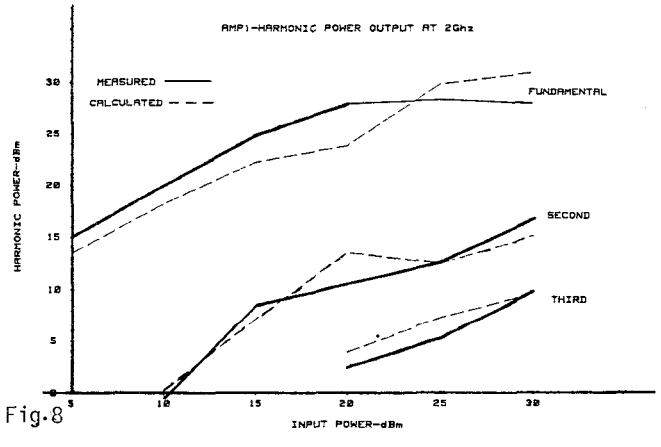


Fig.8

Figure 8: Distributed Power Amplifier Harmonic Power Output at 2 GHz.

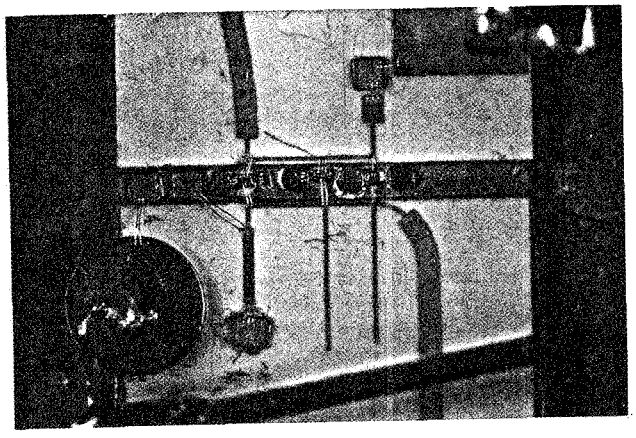


Figure 5: PAMP1 Distributed Power Amplifier

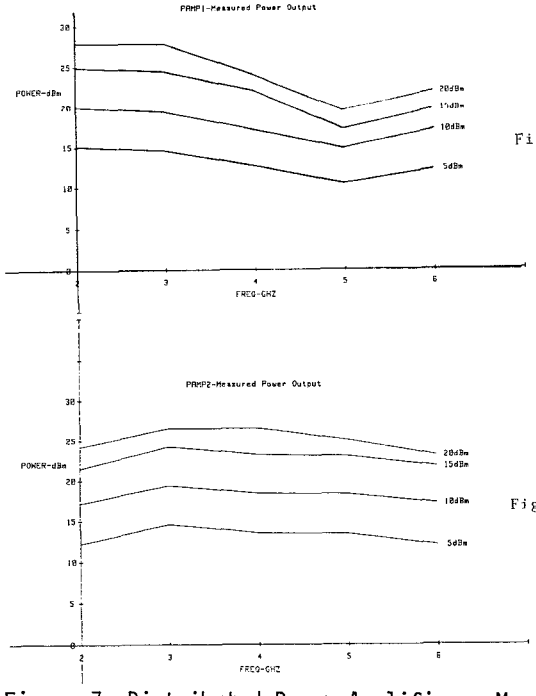


Figure 7a

Figure 7b

Figure 7: Distributed Power Amplifier - Measured Power Output

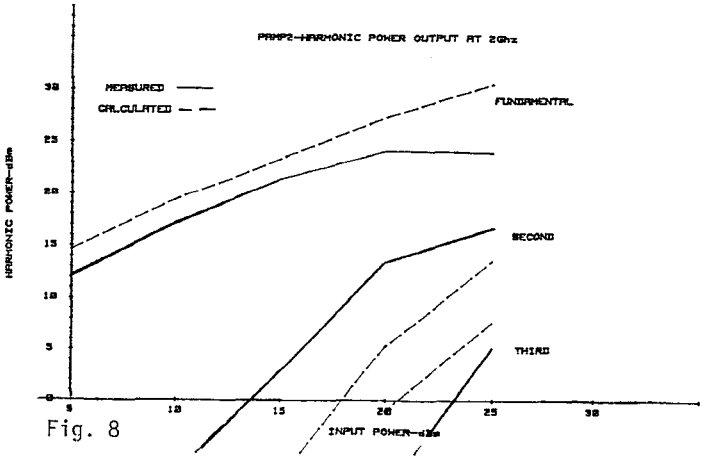


Fig. 8